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of

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for

INTERCONNECT STRUCTURE WITH INTERLAYER DIELECTRIC

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1. Related Applications

This is a divisional US Patent Application Serial No. 09/143,289, filed on August 28, 1998, titled "PLASMA TREATMENT OF AN INTERCONNECT SURFACE DURING FORMATION OF AN INTERLAYER DIELECTRIC ", which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

2. The Field of the Invention

The present invention relates to semiconductor chip processing. More particularly, the present invention relates to formation of interlayer dielectrics that cover electrically conductive interconnects. In particular, the present invention relates to a method of resisting oxidation from the top surface of an electrically conductive interconnect during the formation of an interlayer dielectric.

3. The Relevant Technology

In the microelectronics industry, a substrate refers to one or more semiconductor layers or structures which includes active or operable portions of semiconductor devices. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

Semiconductor chip processing technology involves miniaturizing a plurality of semiconductive devices and placing them side-by-side upon a wafer. As miniaturization technology progresses, it has become expedient to stack semiconductive devices in order to

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retain a small chip footprint. It is also necessary to connect stacked devices by way of formation of an interconnect corridor and by filling of the interconnect corridor with electrically conductive material such as a tungsten stud. Metallization lines are formed that make electrical connection to the tungsten stud. These metallization lines need to be electrically isolated from semiconductive devices that are formed above an existing layer of semiconductive devices. To this end, an interlayer dielectric (ILD) such as an oxide or nitride is formed.

Figure 1 is an elevational cross-section view of a semiconductor structure 10 that depicts interconnects 12 within a dielectric layer 14. Semiconductor structure 10 has an upper surface 16 upon which an interlayer dielectric (ILD) layer 18 has been formed. The left half of Figure 1 depicts an initial effect of formation of ILD layer 18 according to the prior art. It can be seen that the portion of interconnect 12 that was exposed as part of upper surface 16 of semiconductor structure 10 has formed an oxide husk 20 upon interconnect 12. Oxide husk 20 is formed either after planarization to form upper surface 16, such as by chemical-mechanical planarization (CMP) or during the deposition of ILD layer 18. Where interconnect 12 is a tungsten plug, oxide husk 20 forms into tungsten oxide (WO_3).

Further processing of semiconductor structure 10, including thermal processing, causes complications that arise in the prior art. The right half of Figure 1 depicts one prior art problem. It can be seen that, due to a large stress between oxide husk 20 and interconnect 12, oxide husk 20 has delaminated from interconnect 12 due to adhesion failure, and pushed upwardly to form a void 22 immediately above interconnect 12. Void 22 causes planarity problems and can also lead to underetched trenches prior to metal fill. The delamination of oxide husk 20 is an indication of a relatively thick oxide over interconnect 12. The thickness of oxide husk can range from about 10Å to about 500Å. Oxide husk 20 needs to be removed prior to deposition of a metal line. The presence of void 22 causes a prominence in the ILD topology. The prominence can lead to underetched trenches prior to metal fill, resulting in

the metal line not making sufficient electrical contact with interconnect 12. In addition, the prominence caused by the formation of void 22 can be formed during ILD deposition. Additionally, the prominence formed due to void 22 could cause some imaging problems because of a departure from substantial planarity of the upper surface of the ILD.

The delamination of oxide husk 20 from upper surface 16 immediately above interconnect 12 creates significant yield problems and device failure both during device testing and in the field.

What is needed in the art is a method of overcoming the prior art problems. What is also needed in the art is a method of forming an ILD layer without the formation of an oxide husk and the subsequent formation of a void between the top of the interconnect and the ILD layer. What is needed in the art is a method of preventing or reducing the oxidation of the upper surface of a metallic interconnect during the formation of an interlayer dielectric.

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SUMMARY OF THE INVENTION

The present invention relates to the formation of an ILD layer while preventing or reducing oxidation of the upper surface of an electrically conductive interconnect or contact. Prevention or reduction of oxidation of the upper surface of an interconnect or contact is achieved according to the present invention by passivating the exposed upper surface of the interconnect or contact prior to formation of the ILD. It is to be understood that "interconnect" and "contact" can be interchangeable in the inventive method and structures.

In order to avoid the oxidation of an upper surface of an interconnect during the formation of an ILD layer, an *in situ* passivation of the upper surface of the interconnect, immediately prior to or simultaneously with the formation of the ILD layer, avoids the problems of the prior art.

A preferred embodiment of the present invention comprises providing a semiconductor structure including a dielectric layer. Following the formation of the dielectric layer, a depression is formed in the dielectric layer. The depression terminates at an electrically conductive structure therebeneath. The depression is then filled with an interconnect that is composed of an electrically conductive material, such as a refractory metal, and preferably tungsten. After filling of the depression with the interconnect, an upper surface of the interconnect and dielectric layer is formed by a method such as chemical-mechanical planarization (CMP).

Following the formation of the upper surface, a chemical composition is reacted with at least one monolayer of the upper surface of the interconnect to form a chemical compound having a higher resistance to oxidation than the interconnect.

Preferably, the chemical composition will be a nitrogen-containing chemical compound such as ammonia, NH_3. Where the interconnect is a refractory metal, such as tungsten, the at least one monolayer forms a tungsten nitride-type composition or adsorbed complex. Following formation of the at least one monolayer upon the upper surface of the

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interconnect, formation of the ILD layer may be carried out by such methods as a deposition by the decomposition of tetra ethyl ortho silicate (TEOS), or by chemical vapor deposition (CVD) of oxides, nitrides, carbides, and the like.

In order to form an ILD layer using lower processing temperatures, it is preferred that a CVD be carried out under plasma-enhanced (PE) conditions, *i.e.*, PECVD.

Formation of the ILD layer may be carried out in a manner that introduces materials to form the ILD layer simultaneously with the introduction of the ammonia plasma to create a passivation layer upon the upper surface of the interconnect.

Next, formation of the ILD layer with substantially like materials is carried out under conditions where the ILD layer substantially absorbs the passivation layer and the passivation layer is sufficiently thick to resist substantial formation of the oxide husk.

Alternative compositions to ammonia may be used during plasma treatment of the upper surface of the interconnect. For example, nitrogen-containing compositions that are preferred for the inventive method include ammonia, diatomic nitrogen, nitrogen-containing silane, and the like.

These and other features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is an elevational cross-section view of a semiconductor structure comprising a dielectric layer and a metallic interconnect according to the prior art. It can be seen in Figure 1 that two stages of processing are illustrated, whereby an oxide husk upon the interconnect expands to create a void and a substantially non-planar topology for subsequently deposited layers.

Figure 2 is an elevational cross-section view of a semiconductor structure being manufactured according to the inventive method, where a contact corridor has been opened in a dielectric layer and a liner layer has been deposited upon the dielectric layer and within the contact corridor.

Figure 3 is an elevational cross-section view of the semiconductor structure depicted in Figure 2 after further processing, wherein a metal nitride layer has been formed upon the liner layer, an electrically conductive stud or interconnect has been filled into the depression, and wherein an upper surface has been created by a technique such as planarization. The upper surface includes both the dielectric layer and the interconnect, and wherein a passivation layer has been formed upon the upper surface.

Figure 4 is an elevational cross-section view of the semiconductor structure depicted in Figure 3 after further processing, wherein an ILD layer has been formed upon the upper

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surface according to the inventing methods such that the passivation layer has substantially protected the electrically conductive stud such that oxidation has been substantially resisted.

Figure 5 is an elevational cross-section view of the semiconductor structure depicted in Figure 4 after further processing, wherein a second depression has been formed into the ILD layer according to damascene technology in order to allow a metallization trench to be formed, or an upper level contact to be electrically connected to the interconnect that is beneath the ILD layer.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made to the drawings wherein like structures will be provided with like reference designations. It is to be understood that the drawings are diagrammatic and schematic representations of the embodiment of the present invention and are not drawn to scale.

The present invention relates to the formation of an ILD layer while preventing or reducing oxidation of the upper surface of an interconnect or contact stud. Prevention or reduction of oxidation of the upper surface of an interconnect is achieved according to the present invention by passivating the exposed upper surface of the interconnect prior to formation of the ILD.

In reference to Figure 2, prevention or reduction of the likelihood of oxidation of upper surface 16 of interconnect 12 is accomplished during the formation of ILD layer 18. This is carried out by an *in situ* passivation of upper surface 16 of interconnect 12, immediately prior to or simultaneously with the formation of ILD layer 18, avoids the problems of the prior art.

A preferred embodiment of the present invention, illustrated beginning at Figure 2, comprises providing semiconductor structure 10 consisting of dielectric layer 14. Following the formation of dielectric layer 14, a depression 26 is formed in dielectric layer 14 so as to terminate at an electrically conductive structure therebeneath such as a substrate 24. Depression 26 is then filled with an interconnect 12 as seen in Figure 3, composed of an electrically conductive material such as a refractory metal. Interconnect 12 can be a tungsten stud or the like. After filling of depression 26 with an electrically conductive material, upper surface 16 of interconnect 12 and upper surface 16 of dielectric layer 14 is formed by a method such as CMP as illustrated in Figure 3.

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Following the formation of upper surface 16, a chemical composition is reacted with at least one monolayer of upper surface 16 of interconnect 12 to form a chemical compound having a higher resistance to oxidation than interconnect 12.

The chemical compound is provided in an amount sufficient to substantially chemically cover upper surface 16 of interconnect 12 in order to chemically protect approximately the first 1-1,000 atomic lattice layers thereof. The chemical compound may be a nitride form of the metal of which interconnect 12 is composed. Where ammonia, a hydrated nitrogen compound or the like is used, a chemical structure such as $M-N-H_x$, where M represents the metal of which interconnect 12 is composed.

The chemical compound may be, by way of non-limiting example, the nitrogen-containing chemical compound such as ammonia that has been adsorbed onto upper surface 16 of interconnect 12 sufficiently to substantially chemically cover or "blind off" substantially any chemically reactive portion of upper surface 16 of interconnect 12 during formation of ILD layer 18. Use of preferred chemical compounds that are to be matched with specific materials comprising interconnect 12 can be selected by one of ordinary skill in the art using such data and equations as Langmuir's monolayer adsorption isotherm or those also taught by Brunauer, Emmett, or Teller. Of interest to selection of a particular chemical compound in connection with a preferred material for interconnect 12, will be any one of the five types of adsorption isotherms as classified by Brunauer[1].

It is of interest in the present invention that the formation of a passivation layer 32, as seen in Figure 3, substantially protects upper surface 16 of interconnect 12 from oxidation to a degree wherein the formation of oxide husk 20 and void 22 are substantially eliminated. Passivation layer 32 may be achieved by formation of a chemical compound upon upper surface 16 of interconnect 12 by a chemical reaction with approximately the first 1-1,000

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[1] O. Hougen *et al.*, *Chemical Process Principles 2nd Ed., Chapter 10: Adsorption*, John Wiley and Sons, Inc. (1954).

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atomic lattice layers of interconnect 12 or it may be achieved by adsorption onto upper surface 16 of interconnect 12 according to any of the aforementioned types as taught by Brunauer.

Preferably, the chemical composition will be a nitrogen-containing chemical compound such as ammonia, NH_3. Where interconnect 12 is a tungsten stud, the at least one monolayer reacts to form a tungsten nitride-type composition or adsorbed complex upon the at least one monolayer. Following reaction with the at least one monolayer of upper surface 16 of interconnect 12, formation of ILD layer 18 may be carried out by various methods. One method is deposition by the decomposition of tetra ethyl ortho silicate (TEOS), or by CVD of oxides, nitrides, carbides, and the like.

In order to form ILD layer 18 using lower processing temperatures, it is preferred that a CVD be carried out under plasma-enhanced conditions, *i.e.*, PECVD. According to the inventive method, PECVD temperatures are used in a temperature range from about 100°C to about 600°C. Preferably, the processing temperature will be in a range from about 150°C to about 500°C, more preferably from about 200°C to about 450 C, and most preferably 300°C to about 400°C.

According to the present invention, a first example is set forth below. Following the formation of dielectric layer 14, as illustrated in Figure 2, depression 26 such as a contact corridor is formed therein, exposing semiconductor substrate 24 that may be, by way of non-limiting example, a metallization line. Following the exposure of semiconductor substrate 24, a titanium liner layer 28 or the like is formed within depression 26. Subsequently, a titanium nitride layer 30 or the like is formed upon titanium liner layer 28. Titanium nitride layer 30 may be formed by thermal nitridation of a portion of titanium liner layer 28, by deposition of titanium nitride thereupon, or by a combination thereof.

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Interconnect 12 is next formed within depression 26. A preferred material for interconnect 12 is tungsten or the like. Tungsten or the like may be formed within depression 26 by CVD, PECVD, or by physical vapor deposition (PVD).

Upper surface 16 as seen in Figure 3, may be formed by such methods as CMP or an anisotropic etchback that has an etch recipe selectivity that is substantially the same for interconnect 12 as for dielectric layer 14. By "substantially the same", it is meant that selectivity favors leaving dielectric layer 14, and favors it over interconnect 12 in a range from about 1.5:1, preferably about 1.2:1, more preferably 1.1:1, and most preferably 1.05:1.

Passivation of upper surface 16 of interconnect 12 is next carried out by placing semiconductor structure 10 within a tool such as a PECVD chamber and introducing and striking an ammonia plasma or the like therein. Treatment temperatures, as set forth above, are imposed upon semiconductor structure 10. The plasma treats upper surface 16 for a time treatment in a range from about 1 to about 60 seconds, preferably from about 5 to about 45 seconds, more preferably from about 20 to about 40 seconds, and most preferably for about 30 seconds.

Formation of ILD layer 18, as illustrated in Figure 4, may be carried out in a manner that introduces materials to form ILD layer 18 simultaneously with the introduction of the ammonia plasma to create a passivation layer 32 upon upper surface 16 of interconnect 12. Alternatively, after the formation of passivation layer 32 has been substantially accomplished, the deposition tool may be substantially evacuated of the ammonia plasma, and dielectric precursor materials may then be introduced to the deposition tool to form ILD layer 18. Other materials may be used to form passivation layer 32 besides ammonia. For example, diatomic nitrogen or a nitrogen-containing silane may be used. The specific material that may be used will depend upon the particular application.

Next, formation of ILD layer 18 with substantially like materials is carried out under conditions where ILD layer 18 substantially absorbs passivation layer 32 and or passivation

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layer 32 is sufficiently thick to resist substantial formation of oxide husk 20. In this embodiment, it is preferred by way of non-limiting example that both passivation layer 32 be formed using NH_3 and ILD layer 18 be formed in a deposition by decomposition of TEOS. Other materials, however, may be chosen.

Completion of this example is carried out by the formation of second depression 34 in ILD layer 18. Accordingly, a masking layer is patterned upon upper surface 36 of ILD layer 18 and an anisotropic etch is carried out to form second depression 34. The etch recipe is selective to interconnect 12 as well as titanium liner layer 28, titanium nitride layer 32, and optionally to dielectric layer 14.

Where formation of passivation layer 32 is carried out at least in part by adsorption, and where ammonia is used by way of non-limiting example, an ammonia compound and its derivatives are substantially adsorbed upon upper surface 16 of interconnect 12. By "substantially adsorbed" it is meant that passivation layer 32 does not volatilize during the time required to form ILD layer 18. This means that volatilization is prevented to an extent that passivation layer 32 resists formation of oxide husk 20, or a portion thereof. Of primary interest in the present invention is the achievement of an embodiment whereby passivation layer 32 sufficiently protects upper surface 16 of interconnect 12 such that during the formation of ILD layer 18, ILD layer sufficiently adheres to upper surface 16 of interconnect 12 without causing structural failure as that experienced in the prior art.

Additionally and preferably, any component of passivation layer 32 that volatilizes during formation of ILD layer 18 will be soluble in the materials that form ILD layer 18 such that no immiscible gas bubbles form from volatilized materials of passivation layer 32.

A second example of the inventive method is set forth below. Semiconductor structure 10 includes dielectric layer 14, made of borophosphosilicate glass (BPSG). Dielectric layer 14 rests upon substrate 24. In this example, substrate 24 can be an electrically conductive film that is typically used to wire semiconductive devices.

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Following the formation of dielectric layer 14, depression 26 is formed by an anisotropic dry etch that stops on substrate 24. The anisotropic dry etch may include such techniques as ion beam milling or an etch recipe that mobilizes a portion of the masking layer such that the masking layer redeposits upon the sidewalls of depression 26 while it is being formed, thereby forming a substantially anisotropic etch.

Following the formation of depression 26, titanium liner layer 28 is deposited upon dielectric layer 14 and substrate 24 preferably by PECVD. Titanium liner layer 28 is then partially treated in a thermal nitride environment in order to grow titanium nitride layer 30 thereupon. Although titanium nitride layer 30 is grown by thermal combination and conversion of a portion of the titanium in titanium liner layer 28 into titanium nitride layer 30, titanium nitride layer 30 may alternatively be formed by deposition of titanium nitride by such techniques as PVD, PECVD, CVD, and the like.

Following the formation of titanium nitride layer 30, interconnect 12 is formed by deposition of tungsten into depression 26. The deposition of tungsten into depression 26 in order to form interconnect 12 may be facilitated by the presence of titanium nitride layer 30 and titanium liner layer 28. Where the formation of interconnect 12 is formed by force-filling of tungsten into depression 26, the presence of titanium nitride layer 30 and titanium liner layer 28 facilitate slippage of the tungsten material along the region of what will become upper surface 16 and into depression 26 so as to fill depression 26.

Following the filling of depression 26 with tungsten or the like in order to form interconnect 12, all tungsten that is not within depression 26 is removed by a technique such as CMP. Because CMP itself may form oxide husk 20, upper surface 16, particularly that portion of upper surface 16 that comprises interconnect 12, may need to be cleaned by such techniques as an interconnect oxide etch that is selective to dielectric layer 14 and unoxidized portions of interconnect 12.

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Following the cleaning of upper surface 16, semiconductor structure 10 is placed within a deposition tool and an ammonia plasma is struck therein. Alternatively, the cleaning of upper surface 16 may be carried out within the same deposition tool where the ammonia plasma is struck. Additionally, the cleaning of upper surface 16 may be carried out within a cluster tool previous to *in situ* transfer of semiconductor structure 10 into the deposition tool. The temperature of semiconductor structure 10 during this stage of the inventive method is in a range substantially the same as in the previous example. Preferably, the treatment time to form passivation layer 32 is less than about 30 seconds. According to this second example, a preferred composition of passivation layer 32 comprises nitrogen that has been adsorbed upon upper surface 16 of interconnect 12 according to Brunauer's Type V adsorption. As a preferred alternative embodiment, upper surface 16 of interconnect 12 is first treated in a nitrogen atmosphere at a temperature sufficient to create tungsten nitride and then under conditions sufficient to create Type V adsorption of several layers of nitrogen compounds upon the tungsten nitride. By several layers of nitrogen compounds, it is understood that the overall composite thickness of passivation layer 32 is about 50Å, preferably about 20Å, more preferably about 10Å, and most preferably about 5Å.

Another example is set forth below. Processing is carried out as set forth in previous examples. The formation of passivation layer 32 is carried out *in situ* with the formation of ILD layer 18. After an optional cleaning of upper surface 16, semiconductor structure 10, within a deposition tool, is fed with a mixture of ammonia and silane or the like. At the beginning of this step of the inventive process, the mixture comprises an ammonia rich feed such that initially passivation layer 32 begins to form upon upper surface 16.

ins B2 The removal of ammonia from the mixture may be carried incrementally. For example, the elimination of ammonia from the mixture may be initiated by decreasing the ammonia portion of the mixture by a preferred percentage of the entire amount of ammonia over a period of time. Specifically, the amount of ammonia may be decreased every five

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seconds by about 5%, such that after about 100 seconds, the amount of ammonia in the feed mixture is reduced to about zero. Alternatively the amount of ammonia may be decreased every five seconds by 10%, such that after about one minute, the amount of ammonia in the feed mixture is reduced to about zero. Alternatively, the amount of ammonia may be decreased by about 25% every five seconds such that after about twenty seconds, the amount of ammonia in the feed mixture has been reduced to about zero. Additionally, the amount of ammonia may be decreased by 50% every five seconds such that after about ten seconds, the amount of ammonia in the feed mixture is reduced to about zero. Finally, the amount of ammonia in the feed mixture may be reduced to about zero after any five-second time increment to about zero from 100% ~~in a single step~~.

As an alternative embodiment and in connection with the reduction of the amount of ammonia in the mixture, processing conditions may be altered from conditions that are less likely to cause formation to oxide husk 20 to conditions that are more likely. For example, processing temperatures sufficient to form passivation layer 32 may be initiated with an ammonia-rich mixture under conditions not likely to cause formation of oxide husk 20. As the amount of ammonia in the mixture is reduced, processing temperatures may be increased proportionally under conditions that are more likely to cause formation of oxide husk 20 than under conditions previously established when the amount of ammonia in the mixture is greater. The initial formation of some of passivation layer 32, however, resists the formation of oxide husk 20. Preferably, the processing temperature will be the same as the deposition temperature for ILD layer 18.

Following the formation of passivation layer 32, upper surface 16 is covered with ILD layer 18 *in situ* by a method as set forth above. During the deposition of ILD layer 18, passivation layer 32 protects upper surface 16 of interconnect 12 and prevents the formation of oxide husk 20. As a preferred alternative embodiment of the present invention, the materials comprising passivation layer 32 may react with ILD layer 18 material without

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causing unwanted oxidation of upper surface 16 of interconnect 12. In this preferred alternative embodiment, the materials comprising passivation layer 32 and ILD layer 18 will interact to form a new compound that will have a lower stress than that of oxide husk 20.

Alternative compositions to ammonia may be used during plasma treatment of upper surface 16 of interconnect 12. For example, nitrogen-containing compositions that are preferred for the inventive method include ammonia, diatomic nitrogen, nitrogen-containing silane, and the like.

Figure 4 illustrates further processing of semiconductor structure 10 as depicted in Figure 3. It can be seen that ILD layer 18 has been formed upon upper surface 16 of semiconductor 10 according to the inventive method. The presence of passivation layer 32 has prevented formation on oxide husk according to an object of the invention. It can be appreciated that passivation layer 32 may form exclusively upon interconnect 12 and alternatively onto titanium liner layer 28 and titanium nitride layer 30. This means that passivation layer 32 may not substantially form upon upper surface 16 over dielectric layer 14 due to incompatible reaction chemistry that prevents any type of reactive material to form.

Following the formation of ILD layer 18, further processing is carried out as illustrated in Figure 5. Second depression 34 is formed into ILD layer 18 by patterning and etching thereof. In a damascene process such as that illustrated in Figure 5, second depression 34 is formed substantially above interconnect 12. Second depression may be, by way of non-limiting example, a wiring trench such that metallization within second depression 34 would run in and out of the plane of Figure 5. Additionally, second depression 34 may be a contact corridor such that metallization would run left to right, substantially within the plane of Figure 5 along the upper surface 36 of ILD layer 18 and filled into second depression such that a metallization line with a contact is formed, whereby the contact is in electrical communication with interconnect 12.

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